TFW GP 2813

PTO/SB/21 (08-00)

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	09/987,607
Filing Date	November 15, 2001
First Named Inventor	Hongyong ZHANG
Group Art Unit	2813
Examiner Name	D. Hogans
Attorney Docket Number	0756-2395

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Declaration and Power of Attorney
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosures
  1. Response to Decision on Petition and Resubmission Under 37 CFR 1.8(b)
  2. Declaration of Adele Stamper
  3. Copy of Stamped Receipt Card
  4. Copy of Amendment
  5. Copy of sample stamped receipt cards with stamp "MELLON"
  6.

Remarks

☒ The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 50-2280 for the above identified docket number.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Eric J. Robinson, Reg. No. 38,285 Robinson Intellectual Property Law Office, P.C. PMB 955 21010 Southbank Street Potomac Falls, VA 20165
Signature	
Date	

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Signature	Rose Fichtel	Date	10-20-05

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Eric J. Robinson, Reg. No. 38,285 Robinson Intellectual Property Law Office, P.C. PMB 955 21010 Southbank Street Potomac Falls, VA 20165
Signature	*Eric J. Robinson*
Date	

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Attorney Docket No. 0756-2395

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OIPE IAP35 OCT 24 2005 PATENT & TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2813
Hongyong ZHANG	)	Examiner: D. Hogans
Serial No. 09/987,607	)	
Filed: November 15, 2001	)	
For: METHOD FOR PRODUCING	)	
SEMICONDUCTOR INTEGRATED	)	
CIRCUIT INCLUDING A THIN FILM	)	
TRANSISTOR AND A CAPACITOR	)	

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Rose Ireland

RESPONSE TO DECISION ON PETITION AND RESUBMISSION

UNDER 37 CFR 1.8(b)

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the *Decision on Petition*, the Applicant respectfully submits this *Resubmission Under 37 CFR 1.8(b)*. Specifically, the Applicant is resubmitting an Amendment as described in greater detail below. Rule 1.8(b) states the following:

> In the event that correspondence is considered timely filed by being mailed or transmitted in accordance with paragraph (a) of this section, but not received in the Patent and Trademark Office, and the application is held to be abandoned or the proceeding is dismissed, terminated, or decided with prejudice, the correspondence will be considered timely if the party who forwarded such correspondence:
>
> (1) Informs the Office of the previous mailing or transmission of the correspondence promptly after becoming aware that the Office has no evidence of receipt of the correspondence;
>
> (2) Supplies an additional copy of the previously mailed or transmitted correspondence and certificate; and
>
> (3) Includes a statement which attests on a personal knowledge basis or to the satisfaction of the Director to the previous timely mailing or transmission. If the correspondence was

sent by facsimile transmission, a copy of the sending unit's report confirming transmission may be used to support this statement.

In accordance with Rule 1.8(b), the Applicant respectfully submits the following:

On February 3, 2004, the Applicant filed the following: *Amendment* and *Certificate of Mailing* for the above (copy attached) (referred to hereinafter as the "Amendment"). The *Amendment* was either deposited with the U.S. Postal Service (USPS) personally by Ms. Adele M. Stamper or was deposited with the USPS by others in the office in the ordinary course of business. Please see the attached *Declaration of Adele M. Stamper* for details regarding the above.

On May 18, 2004, the Patent Office issued a *Notice of Abandonment* indicating "No reply has been received." Upon receipt, Applicant filed a *Petition to Withdraw Holding of Abandonment,* along with a copy of the *Amendment* and *Certificate of Mailing,* along with a receipt card stamped by the Patent Office "MELLON FEB 10 2004."

On October 7, 2005, the Applicant received a *Decision on Petition* indicating that the *Petition to Withdraw Holding of Abandonment* had been denied in that the stamped receipt card provided stamped "MELLON FEB 10 2004" is not a recognized Office date stamp to establish prima facie evidence of receipt.

While it is believed that a PTO stamped receipt card is not required by Rule 1.8(b), it is noted that "MELLON" is in fact a recognized Office date stamp of the Patent Office. In this regard, Applicant attaches copies of receipt cards which have been received in routine course from the Patent Office with a stamp of "MELLON." These stamped receipt cards are for various maintenance fees paid by applicant. Therefore, it is believed that the Patent Office or the U.S. Postal Service likely misdirected the above documents in error to the Maintenance Fee Address used by the PTO. Thus, while these documents may have been received by the wrong office of the U.S. Patent Office, they were nonetheless received by the Patent Office as clearly evidenced by the originally enclosed receipt card.

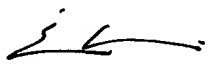
In light of the above facts, it appears that the Amendment and Certificate of Mailing of February 3, 2004, was likely misdirected, either after Ms. Stamper personally deposited the above-referenced documents with the USPS or after the above-referenced documents were deposited with the USPS by others in the office in the ordinary course of business.

The Applicant attaches herewith a true and accurate copy of the *Amendment* and *Certificate of Mailing* filed February 3, 2004. Therefore, the Applicant respectfully submits that the present *Resubmission* is accompanied by a reply required to the outstanding *Office Action.*

No fee is believed to be necessary at this time. However, the Commissioner is hereby authorized to charge fees under 37 CFR §§ 1.16, 1.17, 1.20(a), 1.20(b), 1.20(c), and 1.20(d) (except the Issue Fee) which may be required now or hereafter, or credit any overpayment to Deposit Account No. 50-2280.

Upon entry of the present *Resubmission*, the Applicant respectfully requests that the *Amendment* be entered and acted upon in due course.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

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In re PATENT application of:

MASAKI YOSHIMURA
Serial No. 09/300,598
Filed: 04/28/1999
Due Date: 11/08/2004
For: DISK STOCKER CONTROL AND DISK REPRODUCING APPARATUS
Docket: 0670-0212
November 8, 2004
EJR/EJR/rmf

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OCT 24 2004
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In re PATENT application of:

KAZUYA KOYAMA et al
Serial No. 08/575,752
Filed: 12/20/1995
Due Date: 09/10/2005
For: ROBBERY-PROOF MECHANISM FOR VEHICLE MOUNTED ELECTRONIC APPARATUS
Docket: 0670-0170
August 26, 2005
EJR/EJR/rmf

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In re PATENT application of:

YOSHIO SAKAMOTO
Serial No. 08/731,053
Filed: 10/09/1996
Due Date: 09/30/2005
For: SPEAKER MOUNT STRUCTURE OF VEHICLE
Docket: 0670-0187
August 26, 2005
EJR/EJR/rmf

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Potomac Falls, Virginia 20165

Attorney Docket No. 0756-2395

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2813
Hongyong ZHANG	)	Examiner: D. Hogans
Serial No. 09/987,607	)	
Filed: November 15, 2001	)	
For: METHOD FOR PRODUCING	)	
SEMICONDUCTOR INTEGRATED	)	
CIRCUIT INCLUDING A THIN FILM	)	
TRANSISTOR AND A CAPACITOR	)	

DECLARATION

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I, Adele M. Stamper, a secretary of Robinson Intellectual Property Law Office, P.C., attest as follows:

1. I have reviewed the *Amendment* and *Certificate of Mailing* for the above, all of which correspond with the above-referenced patent application.

2. Specifically, I have reviewed the *Certificate of Mailing* and note that my signature is on the *Certificate of Mailing*.

3. I attest that on February 3, 2004, an *Amendment* and *Certificate of Mailing* of the above was copied, the original document was deposited in an envelope, the envelope was addressed to the Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, the envelope containing the documents was weighed using a postage meter, sufficient First Class postage was applied to the envelope containing the documents, and the stamped envelope containing the documents was either deposited with the USPS personally by me or was deposited with the USPS by others in my office in the ordinary course of business. In the ordinary course of business in my office, all

correspondence to the U.S. Patent & Trademark Office is collected in a central location and is routinely deposited with the USPS.

4. Based on the above, I attest that the *Amendment* and *Certificate of Mailing* of the above was deposited on February 3, 2004, with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to the Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

5. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Respectfully submitted,

Adele M. Stamper

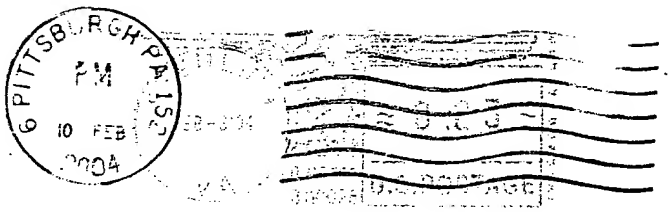
Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789

This will acknowledge receipt of the following:

1. Amendment
2. Certificates of Mailing for each of the above

In re PATENT application of:

HONGYONG ZHANG
Serial No. 09/987,607
Filed: 11/15/2001
Due Date: 02/03/2004
For: METHOD FOR PRODUCING SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING A THIN FILM TRANSISTOR AND A CAPACITOR
Docket: 0756-2395
February 3, 2004
EJR/EJR/ams



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Robinson Intellectual Property Law Office
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165

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Attorney Docket No. 0756-2395

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
Hongyong ZHANG)
Serial No. 09/987,607)
Filed: November 15, 2001)
For: METHOD FOR PRODUCING)
SEMICONDUCTOR INTEGRATED)
CIRCUIT INCLUDING A THIN FILM)
TRANSISTOR AND A CAPACITOR)

Group Art Unit: 2813
Examiner: D. Hogans

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 2.3.2004.
Adele M Stamper

AMENDMENT

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Official Action dated November 3, 2003, please consider the following amendments and remarks in connection with the above-identified application.

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 9 of this paper.

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming an interlayer insulator comprising at least an upper layer comprising silicon nitride and a lower ~~layers~~ layer comprising silicon oxide, each comprising different dry etching characteristics;

etching the upper layer of the interlayer insulator using a first mask, wherein the lower layer of the interlayer insulator is used as an etching stopper;

forming a second mask to cover a portion of the lower layer of the interlayer insulator, which is exposed by the etching step; and

selectively etching the lower layer of the interlayer insulator using the second mask to form a contact hole.

2. (Currently Amended) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a first conductive film on a gate insulating film;

patterning the first conductive film to form a gate electrode;

forming an interlayer insulator comprising at least two layers on the gate insulating film;

forming a first contact hole by removing a part of an upper layer of the interlayer insulator, the part being located over at least one of a source region and a drain region;

forming a second contact hole overlapped with the first contact hole through the interlayer insulator to reach at least one of the source region and the drain region;

forming a second conductive film;

patterning the second conductive film to form a pixel electrode;

forming a third conductive film; and

patterning the third conductive film to form at least one of a source electrode and a drain electrode, which is in electrical contact with the pixel electrode.

3. (Currently Amended) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a first conductive film comprising aluminum on a gate insulating film;

patterning the first conductive film to form a gate electrode;

forming an interlayer insulator comprising at least two layers on the gate insulating film;

forming a first contact hole by removing a part of an upper layer of the interlayer insulator, the part being located over at least one of a source region and a drain region;

forming a second contact hole overlapped with the first contact hole through the interlayer insulator to reach at least one of the source region and the drain region;

forming a second conductive film;

patterning the second conductive film to form a pixel electrode;

forming a third conductive film; and

patterning the third conductive film to form at least one of a source electrode and a drain electrode, which is in electrical contact with the pixel electrode.

4. (Currently Amended) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a first conductive film on a gate insulating film;

patterning the first conductive film to form a gate electrode;

forming an interlayer insulator comprising at least two layers on the gate insulating film;

forming a first contact hole by removing a part of an upper layer of the interlayer insulator, the part being located over at least one of a source region and a drain region;

forming a second contact hole overlapped with the first contact hole to reach at least one of the source region and the drain region;

forming a second conductive film;

patterning the second conductive film to form a pixel electrode;

forming a third conductive film; and

patterning the third conductive film to form at least one of a source electrode and a drain electrode, which is in electrical contact with the pixel electrode,

wherein the contact hole is formed smaller than the part.

5. (Currently Amended) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a first conductive film on a gate insulating film;

patterning the first conductive film to form a gate electrode;

forming an interlayer insulator on the gate insulating film;

forming a first contact hole by removing a part of the interlayer insulator, the part being located over at least one of a source region and a drain region;

forming a second contact hole overlapped with the first contact hole through the interlayer insulator to reach at least one of the source region and the drain region;

forming a second conductive film;

patterning the second conductive film to form a pixel electrode;

forming a third conductive film; and

patterning the third conductive film to form at least one of a source electrode and a drain electrode, which is in electrical contact with the pixel electrode.

6. (Canceled)

7. (Original) The method according to claim 2 wherein the interlayer insulator comprises at least one of silicon oxide film and silicon nitride film.

8. (Original) The method according to claim 3 wherein the interlayer insulator comprises at least one of silicon oxide film and silicon nitride film.

9. (Original) The method according to claim 4 wherein the interlayer insulator comprises at least one of silicon oxide film and silicon nitride film.

10. (Original) The method according to claim 5 wherein the interlayer insulator comprises at least one of silicon oxide film and silicon nitride film.

11. (Original) The method according to claim 2 wherein the pixel electrode comprises indium tin oxide.

12. (Original) The method according to claim 3 wherein the pixel electrode comprises indium tin oxide.

13. (Original) The method according to claim 4 wherein the pixel electrode comprises indium tin oxide.

14. (Original) The method according to claim 5 wherein the pixel electrode comprises indium tin oxide.

15. (Original) The method according to claim 2 wherein the gate electrode is anodized.

16. (Original) The method according to claim 3 wherein the gate electrode is anodized.

17. (Original) The method according to claim 4 wherein the gate electrode is anodized.

18. (Original) The method according to claim 5 wherein the gate electrode is anodized.

19. (Original) The method according to claim 1 wherein the semiconductor device is a liquid crystal display device.

20. (Original) The method according to claim 2 wherein the semiconductor device is a liquid crystal display device.

21. (Original) The method according to claim 3 wherein the semiconductor device is a liquid crystal display device.

22. (Original) The method according to claim 4 wherein the semiconductor device is a liquid crystal display device.

23. (Original) The method according to claim 5 wherein the semiconductor device is a liquid crystal display device.

24. (Currently Amended) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a first interlayer insulating film on a surface;

forming a second interlayer insulating film on the first interlayer insulating film wherein the second interlayer insulating film has a different etching characteristic from the first interlayer insulating film;

forming [[an]] a first opening in the second interlayer insulating film by first etching to expose a surface of the first interlayer insulating film wherein the first interlayer insulating film functions as an etching stopper during the first etching; and

forming [[an]] a second opening in the first interlayer insulating film by second etching the exposed surface of the first interlayer insulating film,

wherein the second interlayer insulating film is ~~at least five times thicker~~ 1/5 to 1/50 thinner than a total thickness of the first interlayer insulating film and the second interlayer insulating film.

25. (Previously Presented) The method according to claim 24 wherein the first interlayer insulating film comprises silicon oxide and the second interlayer insulating film comprises silicon nitride.

26. (Previously Presented) The method according to claim 24 wherein the semiconductor device is a liquid crystal device.

27. (Currently Amended) A method for manufacturing a semiconductor device comprising at least one thin film transistor, comprising the steps of:

forming a semiconductor island on an insulating surface;

forming a gate insulating film comprising silicon oxide on the semiconductor island;

forming a gate electrode over the semiconductor island with the gate insulating film interposed therebetween;

forming a first insulating film comprising silicon oxide over the gate insulating film and the gate electrode;

forming a second insulating film comprising silicon nitride on the first interlayer insulating film;

first etching the second insulating film to form an opening wherein the first insulating film functions as an etching stopper;

second etching a portion of the first insulating film and the gate insulating film in accordance with the opening of the second insulating film, thereby, exposing a surface of the semiconductor layer,

wherein the second interlayer insulating film is ~~at least five times thicker~~ 1/5 to 1/50 thinner than a total thickness of the first interlayer insulating film and the second interlayer insulating film.

28. (Previously Presented) The method according to claim 27 wherein the semiconductor device is a liquid crystal device.

REMARKS

The Official Action mailed November 3, 2003, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on November 15, 2001, and September 20, 2002.

Claims 1-29 were pending in the present application prior to the above amendment. The Applicant notes with appreciation the allowance of claims 2-5, 7-18 and 20-23 (page 14, Paper No. 17). Claim 6 has been canceled, and claims 1-5, 24 and 27 have been amended to better recite the features of the present invention. Accordingly, claims 1-5 and 7-29 are now pending in the present application, of which claims 1-5, 24 and 27 are independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Paragraph 2 of the Official Action rejects claims 1, 6, 24 and 25 as anticipated by JP 62-274729 to Katami. As stated in MPEP § 2131, to establish an anticipation rejection, each and every element as set forth in the claim must be described either expressly or inherently in a single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Katami does not teach all the elements of the independent claims, either explicitly or inherently. The Applicant respectfully submits that an anticipation rejection cannot be maintained against independent claim 1 of the present invention. Claim 1 recites "forming a second mask to cover a portion of the lower layer of the interlayer insulator, which is exposed by the etching step." The Official Action asserts that Katami teaches "forming a second mask (107) to cover a portion of the silicon dioxide layer, which is exposed by the etching step" (page 3, Paper No. 17, citing Figs. 1A-1G). The Applicant respectfully disagrees and traverses the above assertions. The second mask

107 of Katami does not cover a portion of the lower layer (i.e. the SiO_2 film 105) exposed by an etching step (see Fig. 1E of Katami). Therefore, Katami does not teach forming a second mask to cover a portion of a lower layer of an interlayer insulator, which is exposed by an etching step.

Also, the Applicant respectfully submits that an anticipation rejection cannot be maintained against independent claim 24 of the present invention, as amended. Claim 24 has been amended to recite a relative thickness of first and second interlayer insulating films, which is supported in the specification at page 1, lines 32-35. Specifically, claim 24 recites that a second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of a first interlayer insulating film and the second interlayer insulating film. Katami does not teach that a second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of a first interlayer insulating film and the second interlayer insulating film.

Since Katami does not teach all the elements of the independent claims, either explicitly or inherently, an anticipation rejection cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 102(b) are in order and respectfully requested.

Paragraph 4 of the Official Action rejects claim 1 as anticipated by U.S. Patent No. 5,635,423 to Huang et al. The Applicant respectfully submits that an anticipation rejection cannot be maintained against independent claim 1 of the present invention, as amended. The Applicant has amended claim 1 to include the features of claim 6. Specifically, claim 1 has been amended to recite forming an interlayer insulator comprising at least an upper layer comprising silicon nitride and a lower layer comprising silicon oxide, each comprising different dry etching characteristics. The Official Action concedes that Huang does not "explicitly teach wherein the upper/second interlayer insulator is silicon nitride and wherein the lower/first interlayer insulator is silicon oxide" (page 7, Paper No. 17). Therefore, the anticipation rejection of amended claim 1 cannot be maintained.

Since Huang does not teach all the elements of the independent claims, either explicitly or inherently, an anticipation rejection cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 102(e) are in order and respectfully requested.

Paragraph 6 of the Official Action rejects claim 24 as obvious based on Huang. The Applicant respectfully submits that a *prima facie* case of obviousness cannot be maintained against the independent claims of the present invention, as amended.

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims, as amended. As noted above, claim 24 has been amended to recite that a second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of a first interlayer insulating film and the second interlayer insulating film. Huang does not teach or suggest that a second interlayer insulating film is 1/5 to

1/50 thinner than a total thickness of a first interlayer insulating film and the second interlayer insulating film.

Since Huang does not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Paragraph 7 of the Official Action rejects claims 6 and 25 as obvious based on the combination of Huang and Katami. The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims, as amended. Please incorporate the arguments above with respect to the deficiencies in Huang and Katami. Huang and Katami, either alone or in combination, do not teach or suggest forming a second mask to cover a portion of a lower layer of an interlayer insulator, which is exposed by an etching step (claim 1), forming an interlayer insulator comprising at least an upper layer comprising silicon nitride and a lower layer comprising silicon oxide, each comprising different dry etching characteristics (claim 1), or that a second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of a first interlayer insulating film and the second interlayer insulating film (claim 24). Since Huang and Katami do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Paragraph 8 of the Official Action rejects claims 19 and 26-28 as obvious based on the combination of Huang and U.S. Patent No. 5,063,378 to Roach. Paragraph 9 of the Official Action rejects claims 19 and 26-28 as obvious based on the combination of Katami and Roach. Roach does not cure the deficiencies in Huang and Katami. The Official Action relies on Roach to allegedly teach a TFT connected to a pixel electrode (page 9, Paper No. 17). Also, please note, independent claim 27 has been amended in a manner similar to claim 24. Huang, Katami and Roach, either alone or in combination, do not teach or suggest forming a second mask to cover a portion of a

lower layer of an interlayer insulator, which is exposed by an etching step (claim 1), forming an interlayer insulator comprising at least an upper layer comprising silicon nitride and a lower layer comprising silicon oxide, each comprising different dry etching characteristics (claim 1), or that a second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of a first interlayer insulating film and the second interlayer insulating film (claims 24 and 27). Since Huang, Katami and Roach do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Paragraph 10 of the Official Action rejects claim 27 as obvious based on Katami. Katami does not teach or suggest that a second interlayer insulating film is 1/5 to 1/50 thinner than a total thickness of a first interlayer insulating film and the second interlayer insulating film (claim 27). Since Katami does not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

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